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| 10/828,910 | 04/21/2004 | Vincent Nguyen | 200316223-1 | 5643 |

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| EXAMINER | |
|---|---|
| SPITTLE, MATTHEW D | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2111 | |

DATE MAILED: 05/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/828,910 | NGUYEN ET AL. | |
| | Examiner | Art Unit | |
| | Matthew D. Spittle | 2111 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *29 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Response to Arguments*

Applicant's arguments with respect to claims 1- 20 have been considered but are moot in view of the new ground(s) of rejection.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 – 4, 11, 12, and 16 – 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Locker et al.

Regarding claim 1, Locker et al. describe a computer system, comprising:

A central processing unit (CPU) (Figure 1, item 200);

A bridge coupled to the CPU (Figure 1, item 212; connected by memory controller and links 202 and 230);

A first slot configured to receive a device (Figure 1, item 210), wherein a first portion of the bridge is coupled to the first slot (Figure 1 shows slot 210 coupled to the bridge via links 208 and 238);

A second slot configured to receive a device (Figure 2, item "Slot 1"), wherein a second portion of the bridge is coupled to the second slot (Figure 2 shows Slot 1 connected to links 208 and 238 which are linked to the bridge 212);

At least one trace coupled to the first and second slots (Figure 1 and 2, items 208, 238);

Whereby the computer system is configured so that inserting a jumper board (Figure 1 and 2, item 300) in the first slot couples the first portion of the bridge to the second slot while the jumper board does not occupy the second slot (Figure 3 shows how the first slot couples the bridge to a first slot (310) via connections through logic (308)).

Regarding claim 2, Locker et al. describe wherein the first and second portions of the bridge comprise a bus (Figure 1, items 208 and 238 are shown as a PCI bus and an SM bus).

Regarding claim 3, Locker et al. describe wherein each slot is capable of providing all signals pertaining to a bus (column 3, lines 6 – 22).

Regarding claim 4, Locker et al. describe a computer system comprising:

A central processing unit (CPU) (Figure 1, item 200);

A bridge coupled to the CPU (Figure 1, item 212; connected by memory controller and links 202 and 230);

A first slot configured to receive a device (Figure 1, item 210), wherein a first portion of the bridge is coupled to the first slot (Figure 1 shows slot 210 coupled to the bridge via links 208 and 238);

A second slot configured to receive a device (Figure 2, item "Slot 1"), wherein a second portion of the bridge is coupled to the second slot (Figure 2 shows Slot 1 connected to links 208 and 238 which are linked to the bridge 212);

At least one trace coupled to the first and second slots (Figure 1 and 2, items 208, 238);

Whereby the computer system is configured so that inserting a jumper board (Figure 1 and 2, item 300) in the first slot couples the first portion of the bridge to the second slot (Figure 3 shows how the first slot couples the bridge to a first slot (310) via connections through logic (308)), wherein the slots are implemented on a riser board (Figures 1, 2, 3, item 300; column 2, lines 53 – 56).

Regarding claim 11, Locker et al. describe a method of providing a bus in a computer system, comprising:

Routing a first portion of the bus to a first segment (Figure 1, items 208, 238) of a first slot (Figure 1, item 210);

Routing a second portion of the bus (Figure 3, items REQ1/GNT1, REQ3/GNT3) to a first segment of a second slot (Figure 3, item 310);

Coupling a second segment of the first slot to a second segment of the second slot (Figure 3, item 208);

Inserting a jumper board (Figures 1, 2, 3, item 300) into the first slot (Figure 3, item 210);

Wherein the jumper board connects the first and second segments of the first slot (Figure 3, item 210), thereby routing the first portion of the bus (Figure 3, item 208) to the second slot (Figure 3, item 310) while the jumper board (Figure 3, item 300) does not occupy the second slot (Figure 3 shows the jumper board occupying the first slot, 210).

Regarding claim 12, Locker et al. describe wherein the first and second portions of the bus comprise the entire bus (Examiner interprets an entire PCI bus consisting of both the PCI data bus itself and the grant/request signals; Figure 3).

Regarding claim 16, Locker et al. describe wherein the connection between slots occurs on a system board (where a system board may be interpreted as a riser card; Figure 3).

Regarding claim 17, Locker et al. describe a computer system, comprising:

Means for allocating a bus among a first (Figure 3, item 210) and a second slot (Figure 3, item 310);

Means for coupling a portion of the first slot to a portion of the second slot while not occupying the second slot (Figure 3, item 208);

Means for coupling at least two portions of a first slot together (Examiner interprets the slot connector itself coupling two portions of it together; Figure 3, item 210).

Whereby the second slot is capable of providing the entire bus (Examiner interprets an entire PCI bus consisting of both the PCI data bus itself and the grant/request signals; Figure 3).

Regarding claim 18, Locker et al. describe wherein the means for coupling (Figure 3, item 208) a portion of the first slot to a portion of the second slot comprises traces on a system board (Examiner interprets as riser card as a system board; Figure 3, item 300).

Regarding claim 19, Locker et al. describe wherein the means for coupling at least two portions of the first slot together (Figure 3, item 210) comprises a jumper board (Figure 3, item 300).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Locker et al. in view of Intel Corporation.

Regarding claims 5 and 6, Locker et al. fail to teach lane polarity inversion techniques on a printed circuit board that includes first and second slots, and also fails to teach lane reversal techniques on a printed circuit board that includes first and second slots.

Intel Corporation teaches using lane polarity inversion and lane reversal for the purposes of eliminating "bowties" on a printed circuit board (page 7, section 1.2.2 – page 9).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate lane polarity inversion and lane reversal techniques on a printed circuit board that includes the first and second slots for the purpose of reducing and/or eliminating "bowties." This would have been obvious in order to reduce the cost of the PCB by reducing the size, complexity, or number of necessary layers.

* * *

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Locker et al. in view of Shipe.

Regarding claim 7, Locker et al. teach a computer system, comprising:

A central processing unit (CPU) (Figure 1, item 200);

A bridge coupled to the CPU (Figure 1, item 212; connected by memory controller and links 202 and 230);

A first slot configured to receive a device (Figure 1, item 210), wherein a first portion of the bridge is coupled to the first slot (Figure 1 shows slot 210 coupled to the bridge via links 208 and 238);

A second slot configured to receive a device (Figure 2, item "Slot 1"), wherein a second portion of the bridge is coupled to the second slot (Figure 2 shows Slot 1 connected to links 208 and 238 which are linked to the bridge 212);

At least one trace coupled to the first and second slots (Figure 1 and 2, items 208, 238);

Whereby the computer system is configured so that inserting a jumper board (Figure 1 and 2, item 300) in the first slot couples the first portion of the bridge to the second slot (Figure 3 shows how the first slot couples the bridge to a first slot (310) via connections through logic (308)).

Locker et al. fail to teach wherein the first and second portions of the bridge include a serial bus.

Shipe teaches that PCI Express is a serial bus that offers low-cost, scalable performance and achieves a high performance connection between two electronic devices such as a motherboard and a card (column 1, lines 23 – 43).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the serial bus as taught by Shipe into the computer system of Locker et al. for the purpose of achieving a low-cost, scalable, high performance connection between a motherboard and a card.

* * *

Claims 8 – 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Locker et al. in view of Shipe, and further in view of Gehrke et al.

Regarding claim 8, Locker et al. and Shipe fail to teach wherein the serial bus comprises an optical bus.

Gehrke et al. teach using a serial bus that comprises an optical bus (column 3, lines 47 – 56) for the purpose of reducing electromagnetic interference from radiating to other devices, thereby increasing the reliability of the system (column 5, line 65 – column 6, line 12).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to use an optical bus as taught by Gehrke et al. in the system of Locker et al. and Shipe to improve the reliability of the system by reducing

electromagnetic interference between interconnected modular electrical devices (such as expansion cards).

Regarding claim 9, Shipe teaches the additional limitation wherein the serial bus is a PCI-Express bus (column 1, lines 27 – 34).

Regarding claim 10, Locker et al. teach the additional limitation wherein the slots do not provide connections for all signals pertaining to the bus without the jumper board (Examiner notes that since the signal-providing circuitry for the slots (Figure 3, item 308) is located on the jumper board, this limitation is met).

* * *

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Locker et al. in view of PCI Express.

Regarding claim 13, Locker et al. fail to teach selecting the first and second slots from among several available slot configurations to correspond to a maximum number of physical lines of the bus.

PCI Express teaches selecting a slot, from among several available slot configurations, to correspond to a maximum number of physical lines of a bus for the purpose of providing a flexible configuration matched to a particular I/O device's bandwidth and application objectives (section 4.2.4.7.1, pages 166 – 167).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to apply the teachings of PCI Express to the bus of Locker et al. for the purpose of providing a flexible configuration matched to a particular I/O device's bandwidth and application objectives. This would have been obvious in order to accommodate future device requirements, thereby extending the life cycle of the bus.

* * *

Claims 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Locker et al. in view of PCI Express.

Regarding claim 14, Locker et al. fail to teach adjusting the first and second slots such that they can physically accommodate more than just the first and second portions.

PCI Express teaches adjusting a slot such that it can physically accommodate more than just a portion of the bus for the purpose of providing a flexible configuration matched to a particular I/O device's bandwidth and application objectives (section 4.2.4.7.1, pages 166 – 167).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to apply the teachings of PCI Express to the bus of Locker et al. for the purpose of providing a flexible configuration matched to a particular I/O device's bandwidth and application objectives. This would have been obvious in order to accommodate future device requirements, thereby extending the life cycle of the bus.

Regarding claim 15, Locker et al. teach the additional limitation wherein the first and second slots are capable of providing all signals that pertain to the entire bus (Examiner interprets an entire PCI bus consisting of both the PCI data bus itself and the grant/request signals; Figure 3).

* * *

Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Locker et al. in view of Intel Corporation.

Regarding claim 20 Locker et al. fail to teach means for reducing a number of bowtie connections in the system.

Intel Corporation teaches using lane polarity inversion and lane reversal for the purposes of eliminating "bowties" on a printed circuit board (page 7, section 1.2.2 – page 9).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate lane polarity inversion and lane reversal techniques on a printed circuit board that includes the first and second slots for the purpose of reducing and/or eliminating "bowties." This would have been obvious in order to reduce the cost of the PCB by reducing the size, complexity, or number of necessary layers.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew D. Spittle whose telephone number is (571) 272-2467. The examiner can normally be reached on Monday - Friday, 8 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MDS

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